LG Electronics

P300 (P3-Raptor) DataSheet

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LG Electronics, Inc.

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About This Document

Revision History

Document Version	Date	Comment
Rev. A (Preliminary)	Aug 16, 2011	Initial Release
Rev. B (Preliminary)	Oct. 16, 2011	Pin Description / Power
1.0	Jan. 06, 2012	Function Block Diagram Description / Operating Temp / Termal Resistance

Purpose

This Document is the datasheet for P300.

Reference Documents

Conventions

NOTE

The “P3-Raptor” is a pet name of P300.

CAUTION

Abbreviation

The following table defines the abbreviations used in this document.

Abbreviation	Description
WDR	Wide Dynamic Range
OSD	On Screen Display
DSS	Digital Slow Shutter
HS-BLC	Highlight Suppress Backlight Compensation

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1 Introduction

1.1 Description

The P300 is an affordable security camera SoC for CCD image sensor. This chip is a high performance single chip solution that supports the wide dynamic range (WDR) imaging in 960H resolution. The P300 can perform the WDR function, 3D noise reduction, OSD, and Digital Zoom.
The 960H/760H CCD can be connected to the P300 for the WDR function. LG's own WDR image synthesis algorithm is used and its performance is at the state-of-art in the camera system.

The P300 employs Micro-processor, frame memory and Video/Iris DAC not only to simplify the system design, but also to achieve a higher level of performance. The P300 supports both analog and digital video outputs.
In addition to basic camera signal processing functions, it includes an AE/AWB/AF detection circuit and a sync signal generation circuit. This chip also has a built-in microcontroller to realize basic camera control functions such as AE/AWB.

1.2 Features

- **Input : 960H/760H NTSC/PAL CCD sensor (Sony/Sharp)**
- **Output : NTSC/PAL CVBS, ITU-R.656 digital output (36MHz/28.636MHz/28.375MHz)**
- **Serial interface for AFE**
- **12bit video processing**
- **True WDR for dual scan CCD and single scan CCD**
- **3D noise reduction (Control level : 100 steps)**
- **On screen dsplay(OSD) with multi-language (Upto 15 languages)**
- **Digital slow shutter (DSS) or sens-up upto x512**
- **Privacy mask 14 zones (8 rectangels, 4 circles, 2 polygons) with mosaic and transparency**
- **Bad pixel correction (Static: 256 points, dynamic:∞)**
- **Digital zoom with high quality image upto 16x (Full view in picture-in-picture)**
- **Digital effect (H/V Mirror)**
- **Auto exposure, auto white balance**
- **Auto focus (For a dedicated customer only)**
- **On-chip optical detector for AF data**
- **On-chip NTSC/PAL video encoder**
- **On-chip 16bit RISC CPU with 512KB flash memory**
- **On-chip frame memory for 3D noise reduction & digital zoom**
- **On-chip 10bit video and IRIS D/A converter**

- On-chip 8 ADCs for AD keys and photo sensors
- Programmable timing generator
- Motion detection (8 regions) with motion display
- Resolution improvement engine
- Serial communication (UART/I2C/SPI)
- Coaxial communication (Pelco-C)
- Supports external sync - digital line-lock function (Built-in pulse detection & phase comparator)
- True progressive scan (Double scan CCD only)
- 144 pins, 10x10 FBGA package, 0.8mm pitch
- 3.3V / 1.0V operation

1.3 Supported Image Sensors

- Sony CCD sensors

	Single Scan		Dual Scan	
	NTSC	PAL	NTSC	PAL
760H	ICX408	ICX409	ICX212	ICX213
960H	ICX672	ICX673	ICX662	ICX663

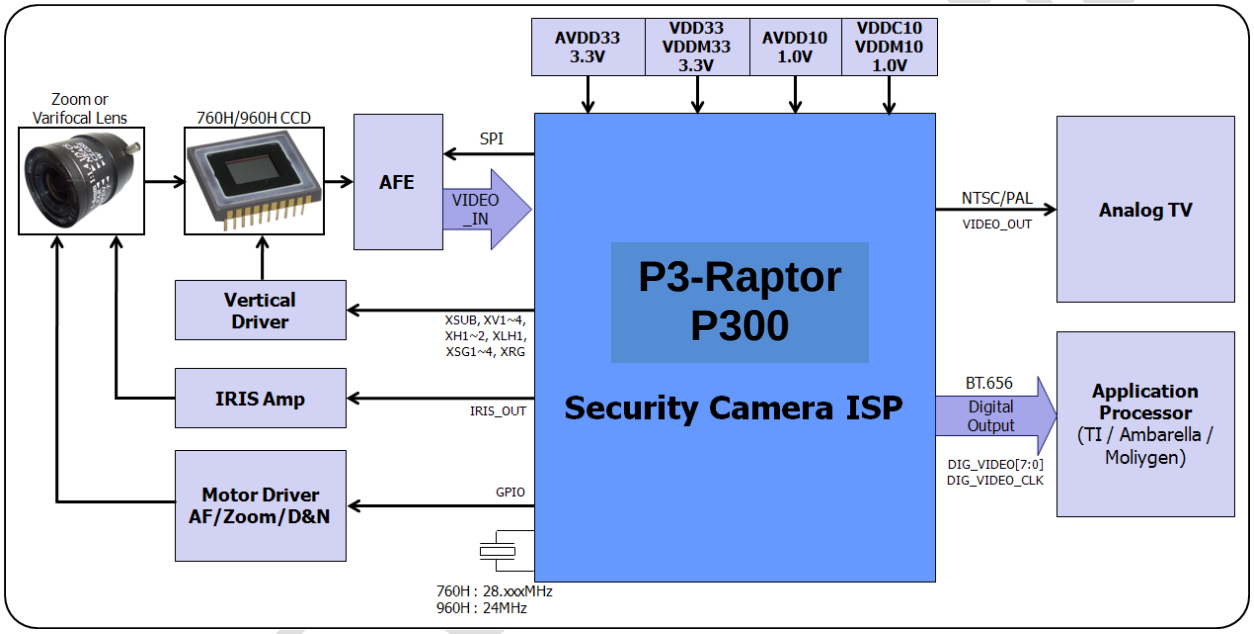
1.4 Applications

- Surveillance CCD Cameras (Box/Dome/Zoom)
- Industrial CCD Cameras (FA)
- Automative CCD Cameras
- Multimedia CCD Cameras (Teleconferencing)

2 Block Diagram

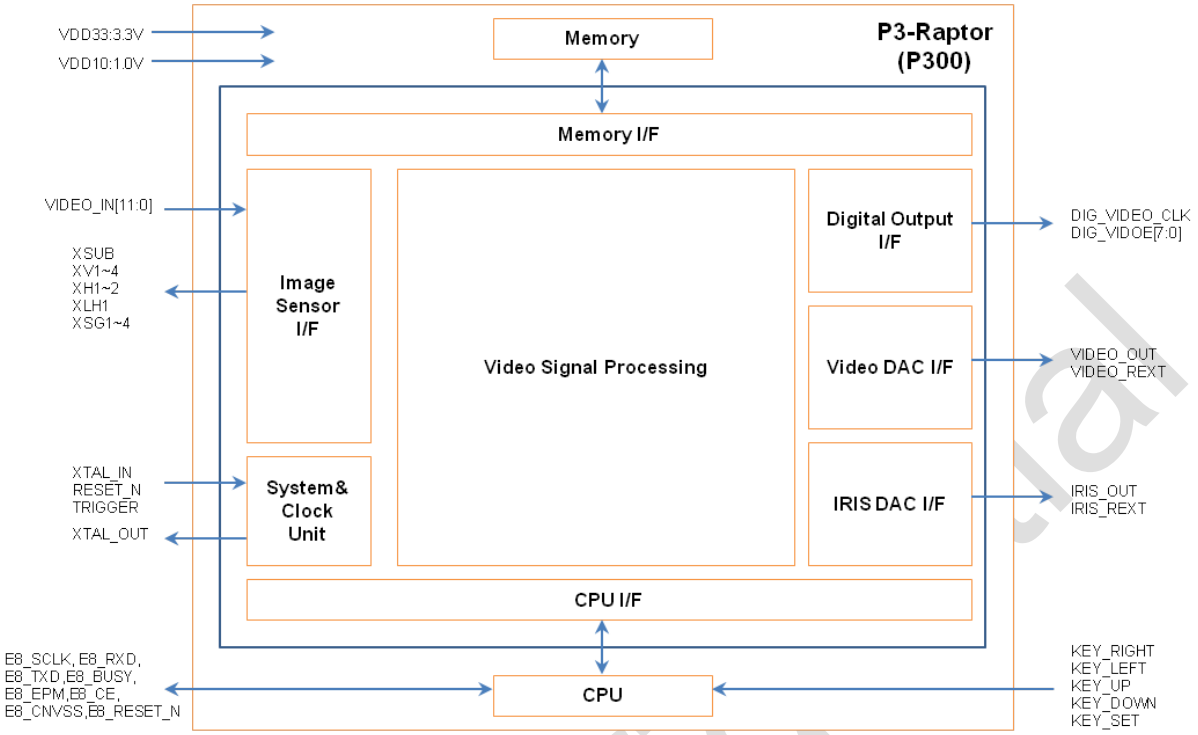
2.1 System Block Diagram

The P300 video-processor is an advanced VLSI device, featuring novel video signal processing techniques for security camera system. The P300 supports 760H/960H CCD image sensors.



[Figure 1] High Resolution Affordable Analog 960H/760H CCD Camera System

2.2 Function Block Diagram



[Figure 2] Function Block Diagram

- **Video Signal Processing**

  The video signal processing block is main core of the P300 to perform digital image processing. Almost novel digital signal processing functions are included in this block. The main functions of the video signal processing block mentioned in the section '1.2 Features'

- **CPU Subsystem**

  The P300 employs 16-bit RISC CPU core. This CPU core performs important task such as AE (Auto exposure), AWB (Auto white balance) and so on.

- **Memory**

  The P300 has memory inside for frame memory of image processing, Some important functions, WDR, Flip, Digital Zoom, 3D DNR and so on.

- **Image Sensor I/F**

  The P300 provides interface to the 760H/960H CCD sensor.

  This interface supports 12-bit data from the CCD sensor with control signals.

  The interface signals:

  - To the vertical driver

    XSUB, XV1, XV2, XV3, XV4, XH1, XH2, XLH1, XSG1, XSG2, XSG3, XSG4, XRG

- To the AFE
  AFE_CS, AFE_SCK, AFE_DOUT, HOPB, PBLK, ADCK, SHP, SHD
- Data Input
  VIDEO_IN[11:0]

- **Digital Output I/F**
  The P300 encodes the digital video signal into a standard NTSC and PAL video signal. The encoder of the P300 performs a low-pass filtering of chrominance and luminance signals to conform to the bandwidth requirements, and performs a digital QAM modulation in order to shift chrominance signals to the sub-carrier frequency and produce a burst signal. It also adds sync and blank signals to the outputs.

- **Video DAC I/F**
  Three 10 bits Digital to Analog Converters (DAC) generate the analog outputs. The encoder of the P300 generates composite (CVBS) format. Alternatively analog Red, Green and Blue signals are generated, with synchronizations signals encoded on the Green line.

- **System & Clock Unit**
  The system & clock unit generates operation clocks for the core clock, DAC clock and clock output.

3 Pin Information

3.1 Pin Configuration

(Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	
A	GND	XSUB	XV1	XV2	XV3	XV4	XH1	XH2	XTAL_IN	XTAL_OUT	RESET_N	GND	A
B	VIDEO_IN_0	VIDEO_IN_1	XLH1	XSG1	XSG2	XSG3	XSG4	XRG	AD_IN_4	AD_IN_6	VIDEO_REXT	VIDEO_OUT	B
C	VIDEO_IN_2	VIDEO_IN_3	EEPROM_DATA	EXT_DN	AD_IN_0	AD_IN_1	AD_IN_2	AD_IN_3	AD_IN_5	AD_IN_7	IDAC_AVDD33	IRIS_REXT	C
D	VIDEO_IN_4	VIDEO_IN_5	EEPROM_CLK	VDD33	GND	GND	VDDC10	VDDM10	PLL_AVDD10	PLL_AVSS10	IDAC_AVSS	IRIS_OUT	D
E	VIDEO_IN_6	VIDEO_IN_7	EN485	VDD33	GND	GND	VDDC10	VDDM10	GND	PLL_AVDD33	VDAC_AVDD33	DN_FWD	E
F	VIDEO_IN_8	VIDEO_IN_9	E8_RESET_N	VDD33	GND	GND	VDDC10	VDDM10	GND	PLL_AVSS33	VDAC_AVSS	DN_REV	F
G	VIDEO_IN_10	VIDEO_IN_11	GPIO_1	VDD33	GND	GND	VDDC10	VDDM10	GND	KEY_UP	E8_EPM	GPIO_3	G
H	HOPB	ADCK	KEY_LEFT	VDDM33	GND	GND	VDDC10	GND	GND	UART_TX	UART_RX	GPIO_2	H
J	PBLK	AFE_CS	E8_CNVSS	VDDM33	GND	GND	VDDC10	GND	GND	E8_BUSY	DIG_VIDEO_7	DIG_VIDEO_CLK	J
K	SHP	AFE_SCK	TRIGGER	TEST_MODE	KEY_SET	IR_ON	I2C_SDA	E8_CE	DSP_CS_N	E8_SCLK	DIG_VIDEO_5	DIG_VIDEO_6	K
L	SHD	AFE_DOUT	COAX_IN	PLL_CFG960_N	GPIO_0	KEY_DOWN	I2C_SCL	E8_TXD	E8_RXD	DIG_VIDEO_1	DIG_VIDEO_3	DIG_VIDEO_4	L
M	GND	MSPI_CS	MSPI_DO	MD_OUT	KEY_RIGHT	SSPI_CS	SSPI_SCK	SSPI_DI	SSPI_DO	DIG_VIDEO_0	DIG_VIDEO_2	GND	M
	1	2	3	4	5	6	7	8	9	10	11	12	

[Figure 3] Pin Map (Top View)

3.2 Pin Description

3.2.1 General Pin Description

Ball No.	Ball Name	IO	Description
J2	AFE_CS	O	AFE Serial Digital Interface Load Pulse
K2	AFE_SCK	O	AFE Serial Digital Interface Clock Ouput
L2	AFE_DOUT	O	AFE Serial Digital Interface Data Output
H1	HOPB	O	AFE Black Level Clamp Clock Input
J1	PBLK	O	AFE Preblanking Clock Input
H2	ADCK	O	AFE Sampling Clock
K1	SHP	O	AFE CDS Sampling Clock for CCD's Reference Level
L1	SHD	O	AFE CDS Sampling Clock for CCD's Data Level
B1	VIDEO_IN_0	I	Digital Video Input 0 for CCD Signal
B2	VIDEO_IN_1	I	Digital Video Input 1 for CCD Signal
C1	VIDEO_IN_2	I	Digital Video Input 2 for CCD Signal
C2	VIDEO_IN_3	I	Digital Video Input 3 for CCD Signal
D1	VIDEO_IN_4	I	Digital Video Input 4 for CCD Signal
D2	VIDEO_IN_5	I	Digital Video Input 5 for CCD Signal
E1	VIDEO_IN_6	I	Digital Video Input 6 for CCD Signal
E2	VIDEO_IN_7	I	Digital Video Input 7 for CCD Signal
F1	VIDEO_IN_8	I	Digital Video Input 8 for CCD Signal
F2	VIDEO_IN_9	I	Digital Video Input 9 for CCD Signal
G1	VIDEO_IN_10	I	Digital Video Input 10 for CCD Signal
G2	VIDEO_IN_11	I	Digital Video Input 11 for CCD Signal
A2	XSUB	O	CCD substrate clock
A3	XV1	O	CCD vertical transfer clock 1
A4	XV2	O	CCD vertical transfer clock 2
A5	XV3	O	CCD vertical transfer clock 3
A6	XV4	O	CCD vertical transfer clock 4
A7	XH1	O	CCD horizontal transfer clock 1
A8	XH2	O	CCD horizontal transfer clock 2
B3	XLH1	O	CCD horizontal final stage transfer clock
B4	XSG1	O	CCD read out pulse 1
B5	XSG2	O	CCD read out pulse 2
B6	XSG3	O	CCD read out pulse 3
B7	XSG4	O	CCD read out pulse 4
B8	XRG	O	CCD reset gate clock
A9	XTAL_IN	I	X-tal Input (960H : 24MHz, 760H:28.xxxMHz)
A10	XTAL_OUT	O	X-tal Output
A11	RESET_ N	I	System Reset (Active Low)
K4	TEST_MODE	I	Test Mode (Always '0')
L4	PLL_CFG960_N	I	PLL Configuration (960H : Low, 760H : High)
K9	DSP_CS_N	I	(External Pull-up)
K3	TRIGGER	I	Line-lock External Sync Signal

L3	COAX_IN	I	Coaxial Communiation
M6	SSPI_CS	I	Slave SPI Serial Chip Select
M7	SSPI_SCK	I	Slave SPI Serial Clock
M8	SSPI_DI	I	Slave SPI Serial Data In (Slave In)
M9	SSPI_DO	O	Slave SPI Serial Data Out (Slave Out)
M10	DIG_VIDEO_0	O	Digital Video Output 0
L10	DIG_VIDEO_1	O	Digital Video Output 1
M11	DIG_VIDEO_2	O	Digital Video Output 2
L11	DIG_VIDEO_3	O	Digital Video Output 3
L12	DIG_VIDEO_4	O	Digital Video Output 4
K11	DIG_VIDEO_5	O	Digital Video Output 5
K12	DIG_VIDEO_6	O	Digital Video Output 6
J11	DIG_VIDEO_7	O	Digital Video Output 7
J12	DIG_VIDEO_CLK	O	Digital Video Pixel Clock (960H : 36MHz, 760H:28.xxxMHz)
M5	KEY_RIGHT	I	Port Key : Right
H3	KEY_LEFT	I	Port Key : Left
G10	KEY_UP	I	Port Key : Up
L6	KEY_DOWN	I	Port Key : Down
K5	KEY_SET	I	Port Key : Set
H10	UART_TX	O	RS232/485 TXD
H11	UART_RX	I	RS232/485 RXD
E3	EN485	IO	GPIO / RS485 RTS
E12	DN_FWD	O	Day & Night Forward Signal
F12	DN_REV	O	Day & Night Reverse Signal
D3	EEPROM_CLK	O	I2C Eeprom Clock
C3	EEPROM_DATA	IO	I2C Eeprom Data
K6	IR_ON	IO	IR LED (PWN or On/Off)
C4	EXT_DN	I	External Day & Night Input
M4	MD_OUT	IO	Motion Detection
C5	AD_IN_0	AI	GPIO / CDS
C6	AD_IN_1	AI	GPIO / ADKEY
C7	AD_IN_2	AI	GPIO
C8	AD_IN_3	AI	GPIO
B9	AD_IN_4	AI	GPIO
C9	AD_IN_5	AI	GPIO
B10	AD_IN_6	AI	GPIO
C10	AD_IN_7	AI	GPIO
K7	I2C_SDA	IO	GPIO / I2C_SDA / MSPI_DI
L7	I2C_SCL	IO	GPIO / I2C_SCL / MSPI_SCK
M2	MSPI_CS	IO	GPIO / MSPI_CS
M3	MSPI_DO	IO	GPIO / MSPI_DO
L5	GPIO_0	IO	GPIO
G3	GPIO_1	IO	GPIO
H12	GPIO_2	O	GPIO
G12	GPIO_3	IO	GPIO
K10	E8_SCLK	IO	Debug & Download Port
L9	E8_RXD	IO	Debug & Download Port
L8	E8_TXD	IO	Debug & Download Port

J10	E8_BUSY	IO	Debug & Download Port
G11	E8_EPM	IO	Debug & Download Port
K8	E8_CE	IO	Debug & Download Port
J3	E8_CNVSS	IO	Debug & Download Port
F3	E8_RESET_N	I	Debug & Download Port
B12	VIDEO_OUT	AO	CVBS Video Output
D12	IRIS_OUT	AO	IRIS Output
B11	VIDEO_REXT	-	External Resister for Video DAC
C12	IRIS_REXT	-	External Resister for IRIS_DAC

AI = Analog Input, AO = Analog Output, I = Digital Input, O = Digital Output, IO = Digital Bi-direct

[Table 1] Pin Description

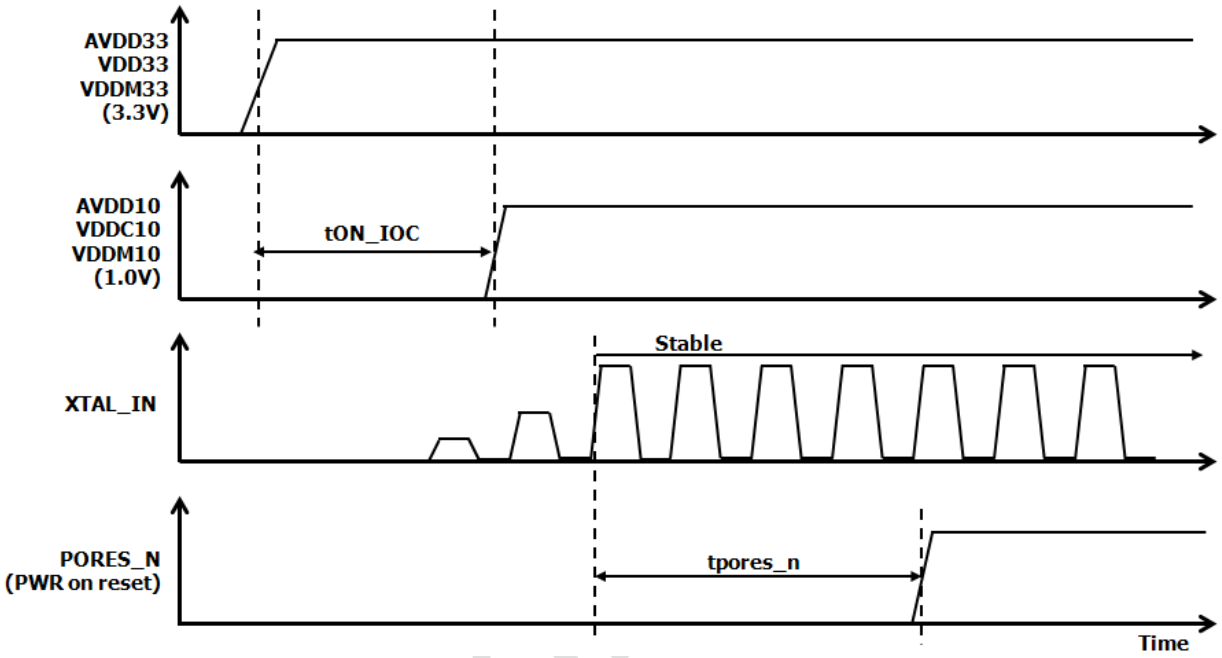
3.2.2 Power Pin Description

Ball No.	Ball Name	IO	Description
E10	PLL_AVDD33	AP	3.3V Analog Power for PLL
D9	PLL_AVDD10	AP	1.0V Analog Power for PLL
F10	PLL_AVSS33	AG	Analog Ground for PLL
D10	PLL_AVSS10	AG	Analog Ground for PLL
E11	VDAC_AVDD33	AP	3.3V Analog Power for Video DAC
F11	VDAC_AVSS	AG	Analog Ground for Video DAC
C11	IDAC_AVDD33	AP	3.3V Analog Power for IRIS DAC
D11	IDAC_AVSS	AG	Analog Ground for IRIS DAC
D7, E7, F7, G7, H7, J7	VDDC10	DP	1.0V Digital Power for CORE1
D8, E8, F8, G8	VDDM10	DP	1.0V Digital Power for CORE2
D4, E4, F4, G4	VDD33	DP	3.3V Digital Power for IO
H4, J4	VDDM33	DP	3.3V Digital Power for CPU
A1, A12, D5, D6, E5, E6, E9, F5, F6, F9, G5, G6, G9, H5, H6, H8, H9, J5, J6, J8, J9, M1, M12	GND	DG	Digital Ground

AP = Analog Power, AG = Analog Ground, DP = Digital Power, DG = Digital Ground

[Table 2] Power Pin Description

4 Power on Sequence



Symbol	Description	Min	Typ	Max
tON_IOC	Core power on time after I/O & Analog power on		> 200 us	
tpores_n	Reset recovery time after stable status of clock and power		> 100 us	

[Figure 4] Power on Sequence Timing Diagram

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
VDDC10 VDDM10	1.0V Digital Power Supply	-0.5		1.3	V
VDD33 VDDM33	3.3V Digital Power Supply	-0.5		4.6	V
PLL_AVDD10	1.0V Analog Power Supply	-0.5		1.3	V
PLL_AVDD33 VDAC_AVDD33 IDAC_AVDD33	3.3V Analog Power Supply	-0.5		4.6	V
VI	Input Voltage	-0.5		VDD33+0.5	V
VO	Output Voltage	-0.5		4.6	V
Tstg	Storage Temperature	-40		125	℃

* Note: Permanent device damage may occur if absolute maximum conditions are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

[Table 3] Absolute Maximum Rating

5.2 Recommended Operating Range

Symbol	Description	Min	Typ	Max	Units
VDDC10 VDDM10	1.0V Power Supply	0.9	1.0	1.1	V
VDD33 VDDM33	3.3V Power Supply	3.0	3.3	3.6	V
PLL_AVDD10	1.0V Analog Power Supply	0.9	1.0	1.1	V

PLL_AVDD33 VDAC_AVDD33 IDAC_AVDD33	3.3V Analog Power Supply	3.0	3.3	3.6	V
Ta	Ambient operating temperature	0		80	℃

[Table 4] Recommended Operating Range

5.3 DC Characteristics

Item	Parameter	Specification			Unit	Related Pin
		Min	Typ	Max		
AIDD	VDDC10		60		mA	
	VDDM10		30			
	VDD33		40			
	VDDM33		50			
	PLL_AVDD33		12			
	PLL_AVDD10		0.4			
	VDAC_AVDD33		35			
	IDAC_AVDD33		17			
SIDD	VDDC10	0		60	mA	
	VDDM10	0		40		
	VDD33	0		100	uA	
	VDDM33	0		240		
	PLL_AVDD33	0		10		
	PLL_AVDD10	0		50		
	VDAC_AVDD33	0		10		
	IDAC_AVDD33	0		10		
V_{IL}	Input Low Voltage	0		0.66	V	
V_{IH}	Input High Voltage	2.64		3.3	V	
V_{OL}	Output Low Voltage			0.5	V	

V_{OH}	Output High Voltage	2.4			V	
I_I	Input Leakage Current @ V_I=3.3V or 0V			±10	uA	
V_T	Threshold Point	1.29	1.39	1.47	V	
V_{T+}	Schmitt Trigger Low to High Threshold Point	1.56	1.67	1.75	V	
V_{T-}	Schmitt Trigger High to Low Threshold Point	1.15	1.23	1.31	V	
Θja	Thermal Resistance (@25℃ , 0.4W)		30.89		℃/W	
Θjc			0.88		℃/W	
Power Consumption (@25℃, 960H CCD)		< 600			mW	

[Table 5] DC Charateristics

5.4 AC Characteristics

5.4.1 Clock Timing

Symbol	Parameter	Min	Typ	Max	Unit	Comments
fclk	XTAL Input Clock Frequency		41.6		ns	XTAL_IN 960 / 24MHz
			34.9		ns	XTAL_IN 760 NTSC / 28.636MHz
			35.2		ns	XTAL_IN 760 PAL / 28.375MHz
fduty	Clock duty cycle	40	50	60	%	

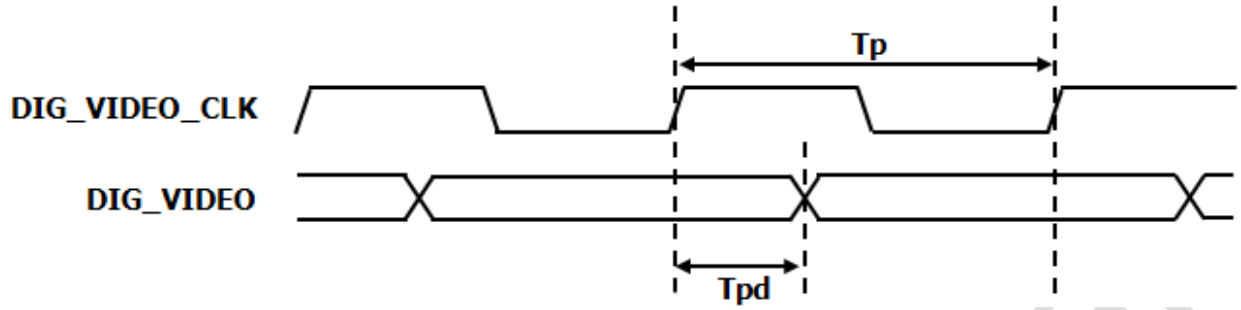
[Figure 5] Clock Timing

5.4.2 Digital Inputs

Symbol	Parameter	Min	Typ	Max	Unit	Comments
All digital inputs						
CI	Input Capacitance		5	-	pF	

[Figure 6] Digital Inputs

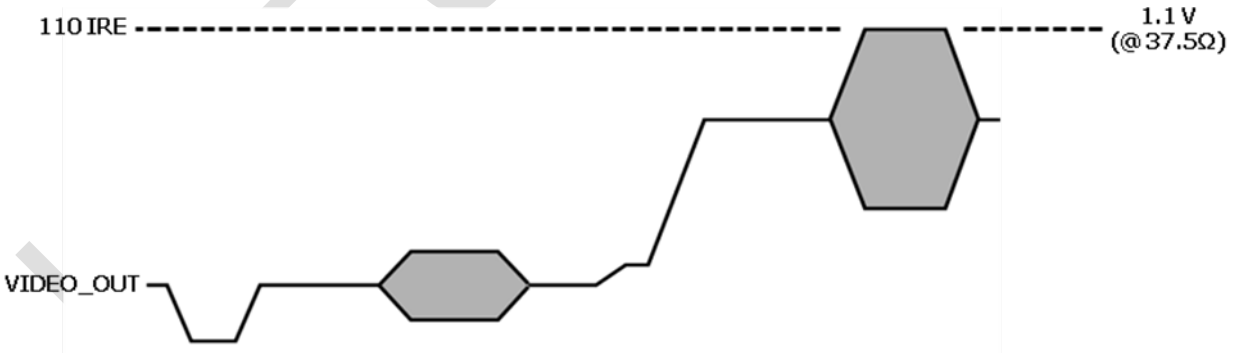
5.4.3 Digital Video Output



Parameter	Min	Typ	Max	Units	Comments
Tp		27.7		ns	960 / 36MHz
		34.9		ns	760 NTSC / 28.636MHz
		35.2		ns	760 PAL / 28.375MHz
Tpd		5		ns	Digital output propagation delay

[Figure 7] Digital Video Output Timing Diagram

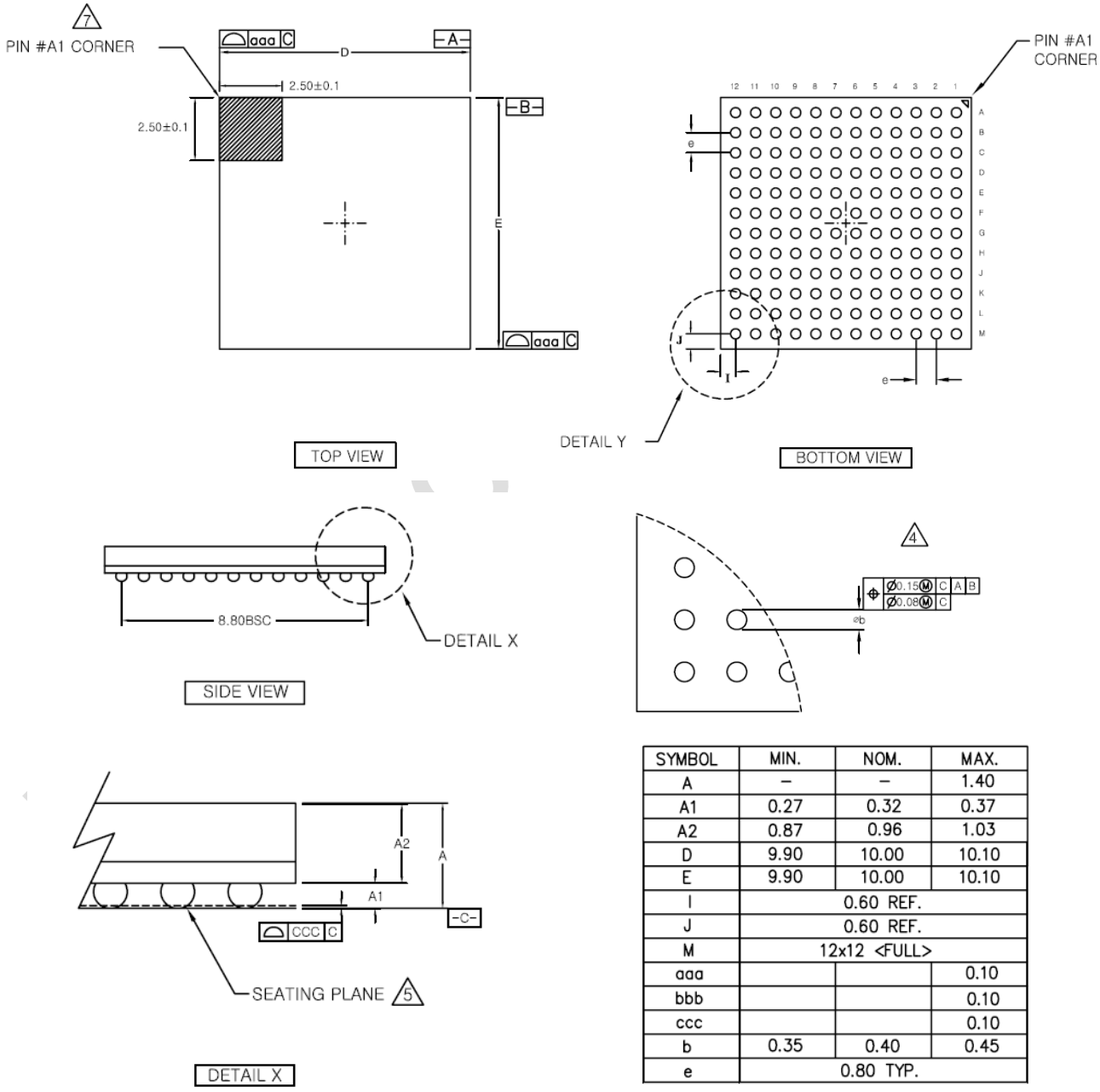
5.4.4 Analog NTSC / PAL Composite Video Output



[Figure 8] Analog NTSC / PAL Composite Video Output Timing Diagram

6 Package Information

Package Type	Ball Pitch	Size
144 FBGA	0.80 mm	10 x 10 mm



SYMBOL	MIN.	NOM.	MAX.
A	–	–	1.40
A1	0.27	0.32	0.37
A2	0.87	0.96	1.03
D	9.90	10.00	10.10
E	9.90	10.00	10.10
I	0.60 REF.		
J	0.60 REF.		
M	12x12 <FULL>		
aaa			0.10
bbb			0.10
ccc			0.10
b	0.35	0.40	0.45
e	0.80 TYP.		

Notes: All linear dimensions are in Millimeters

[Figure 9] Package Dimension